**IN THE SPECIFICATION:**

Please amend the specification as follows:

[0020] FIGS. ~~5A-5G~~ 5A-5F are pictorial representations (through cross sectional views) illustrating alternative processing steps used in forming a high performance semiconductor device containing two NFETs formed on a (100) crystallographic surface, and a PFET, which is located between the NFETs, formed on a (110) crystallographic surface.

[0058] FIGS. 5A-~~5G~~ 5F illustrates alternative processing steps used in forming a high performance semiconductor device containing two NFETs formed on a (100) crystallographic surface, and a PFET, which is located between the NFETs, formed on a (110) crystallographic surface. The alternative method begins with forming the bonded substrate shown in FIG. 5A. The bonded substrate 10 includes at least a surface dielectric layer 18, a first semiconductor layer 16, an insulating layer 14 and a second semiconductor layer 12. A third optional semiconductor layer may be located beneath the second semiconductor layer.

[0062] Oxide is then stripped from the structure shown in FIG. 5F and strained Si 31 is formed on the exposed portions of the first semiconductor layer 16. After forming the strained Si layers, CMOS devices 30 and 32 are formed over the respective crystal orientation that provides a high performance device. ~~The resultant structure containing NFETs and PFETs formed atop strained Si layers is shown, for example, in FIG. 5G.~~